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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/611,307

07/01/2003

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08/01/2007

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EXAMINER

DICKEY, THOMAS L

ART UNIT

PAPER NUMBER

2826

MAIL DATE

DELIVERY MODE

08/01/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Advisory Action</b> <b>Before the Filing of an Appeal Brief</b>	<b>Application No.</b> 10/611,307	<b>Applicant(s)</b> MATSUDA ET AL.	
	<b>Examiner</b> Thomas L. Dickey	<b>Art Unit</b> 2826	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 20 July 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.  
 b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on \_\_\_\_\_. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

#### AMENDMENTS

3. ☒ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because  
 (a) ☒ They raise new issues that would require further consideration and/or search (see NOTE below);  
 (b) ☐ They raise the issue of new matter (see NOTE below);  
 (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or  
 (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: See Continuation Sheet. (See 37 CFR 1.116 and 41.33(a)).

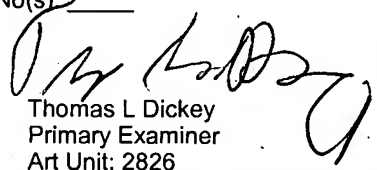
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).  
 5. ☐ Applicant's reply has overcome the following rejection(s): \_\_\_\_\_.  
 6. ☐ Newly proposed or amended claim(s) \_\_\_\_\_ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).  
 7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.  
 The status of the claim(s) is (or will be) as follows:  
 Claim(s) allowed: \_\_\_\_\_.  
 Claim(s) objected to: \_\_\_\_\_.  
 Claim(s) rejected: 1-5 and 15-18.  
 Claim(s) withdrawn from consideration: \_\_\_\_\_.

#### AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).  
 9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing of a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).  
 10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

#### REQUEST FOR RECONSIDERATION/OTHER

11. ☐ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: \_\_\_\_\_.  
 12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08 or PTO-1449) Paper No(s) \_\_\_\_\_.  
 13. ☐ Other: \_\_\_\_\_.

  
 Thomas L. Dickey  
 Primary Examiner  
 Art Unit: 2826

Continuation of 3. NOTE: Proposed Claim 15 is broader than claim 15 as previously searched. As previously searched, claim 15 required "a dummy area on the substrate." This limitation is removed from proposed claim 15. Whether the prior art discloses or suggests a semiconductor area surrounded by a plurality of semiconductor elements not necessarily to be found in a semiconductor area creates a new issue not previously searched or considered.

Also, proposed Claim 15 recites a plurality of semiconductor elements EACH comprising a top electrode and a bottom electrode. This amounts to a recital of a plurality of electrodes, actually two (top and bottom) such pluralities. Likewise, proposed Claim 15 recites a plurality of dummy semiconductor elements EACH comprising a top electrode and a bottom electrode. This amounts to a recital of a plurality of dummy electrodes, actually (again) two such pluralities. It seems to the examiner that the proposed recital of these pluralities of electrodes and dummy electrodes creates a new, §112 issue. On the face of things it appears indefinite which of said plurality of electrodes is referred to by the recital of "the electrode" in line 21. Again, on the face of things it appears indefinite which of said plurality of dummy electrodes is referred to by the recital of "the dummy electrode" in line 21.

The Examiner wishes at this time to point out to Applicant two recent cases, Ex parte CAROLYN RAMSEY CATAN, Appeal 2007-0820, Application 09/734,808 (BPAI, 7/3/07, PRECEDENTIAL) (<http://www.uspto.gov/web/offices/dcom/bpai/prec/fd070820.pdf>) and LEAPFROG ENT. INC. v. FISHER-PRICE, INC., 485 F.3d 1157, 1161, 82 USPQ2d 1687, 1690-91 (Fed. Cir. 2007). CATAN quotes LEAPFROG for the proposition that "The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." CATAN, Slip Op. at 12.

The CATAN panel goes on to say that:

As in LEAPFROG, the device defined by claim 5 is an adaptation of an old invention (Nakano) using newer technology that is commonly available and understood in the art (Harada). Adding bioauthentication to the Nakano device does no more to Nakano's device than it would do if it were added any other device. The function remains the same. Predictably, bioauthentication adds greater security and reliability to an authorization process (FF 12). This variation on Nakano's device, whereby the manual authentication means of the Nakano device is replaced with Harada's bioauthentication means, appears to present no unexpected technological advance in the art. One of ordinary skill in the art of consumer electronic devices would have found it obvious to update the Nakano device with the modern authentication components of the Harada bioauthentication means and thereby gaining, predictably, the commonly understood benefits of such adaptation, that is, a secure and reliable authentication procedure (FF 12).

CATAN, Slip Op. at 18. The Examiner is aware of references demonstrating that when the DRAM industry went to COB (capacitor-over-bitline) configurations, it became commonplace to add "dummy" capacitors on chips, between areas dedicated to DRAM memory. Without these "dummy" capacitors these areas were subject to "dishing" when CMP (chemical-mechanical-polishing) was performed. These "dummy" capacitors were spaced exactly as the real ones were, because spacing between capacitors determined the structures' ability to stand up to the pressure of CMP, just as spacing between steel columns of the first floor of a building determines its ability to stand up to the pressure of floors. These references should already be of record. Likewise, the record should already contain references establishing that high-k or ferroelectric memory capacitors were, at time of Applicants' invention, "newer technology that is commonly available and understood in the art" (borrowing a phrase from the CATAN panel).

In the Examiner's opinion, Applicants' claims will not pass obviousness muster under the CATAN or LEAPFROG standards, if they read on a device that could simply have been produced by combining the known elements of "anti-dishing" dummy capacitors and high-capacity (or non-volatile) high-k or ferroelectric memory capacitors.